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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/528,001	03/17/2000	Shiri Kadambi	P108339-00003	3385

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EXAMINER	
HOANG, THAI D	

ART UNIT	PAPER NUMBER
2668	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/528,001	KADAMBI ET AL.
	Examiner	Art Unit
	Thai D. Hoang	2668

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-2 and 7 are rejected under 35 U.S.C. 102(a) as being unpatentable over Muller et al, US patent No. 5,909,686, hereafter referred to as Muller.

Regarding claims 1 and 7, Muller discloses a network switch stack configuration, which comprises a plurality of switching elements 100, wherein each of elements 100 comprises a plurality of data ports located at network interface 205, a plurality of stacking ports located at a cascading interface 225 for connecting the switching 100 with other switches, and a CPU interface 215; see figures 1-2; col. 3, lines 39-41; col. 4, lines 38-43 (a first network switch comprising a plurality of data ports, a first stacking port, a first internet port interface controller, and a first CPU interface; a second network switch having a plurality of data ports, a second stacking port, a second internet port interface controller and a second CPU interface). In addition, Muller teaches that the network comprises a common CPU 161 connected to each of the interfaces 215 of the switching elements 100 (a common CPU connected to said first CPU interface and said second CPU interface). Muller discloses that the switching elements 100 of subsystems 110 are interconnected to form of cascading as shown in figure 1 by using a number of links 141. Therefore, it indicates that incoming data packets are transmitted/received

from one of the data ports of the switching element 100 to/from any of the data ports of another switching element 100 through the interfaces 225; figures 1-2; col. 4, lines 1-5, 44-57; col. 5, lines 10-21; col. 6, lines 6-30 (the first stacking port and the second stacking port are communicatively connected through said first and second internet port interface controller, such that incoming packets on any of the plurality of data ports on the first and second switches can be effectively switched to any of the plurality of data ports on either of the first and second network switches.) Since switches in the Muller's system are Ethernet packet switches (col.4, lines 44-53); therefore, each of the switch elements 100 in the system shown in figure 1 adds to each of the incoming data packets a Ethernet packet header, which comprises a plurality of header fields, such as source address, destination address, port, IP address.... The switch determines egress port for routing the data packets to a destination according to the information of the headers; col. 13, lines 9-22.

Regarding claim 2, Muller teaches that a central processing system (CPS) 160 that is coupled to the individual subsystem 110 through a communication bus 151. The CPS 160 has a direct control and communication interface to each subsystem 110 and provides some centralized communication and control between switch elements; col. 4, lines 24-34. Furthermore, Muller discloses that the CPU 161 may transmit commands or packets to the network switch element 100 via the CPU interface 215. In this manner, one or more software processes running on the CPU 161 may manage entries in an external forwarding and filtering database 140. It indicates that the CPU 161 is configured to program functions on the switching elements, and controls communication

between switching elements (common CPU is configured to program functions on the first and second network switch, and wherein the common CPU controls communication between the first and second network switch.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al, US patent No. 5,909,686, in view of Muller et al, US Patent No. 6,119,196, hereafter referred to as 686 and 196.

Regarding claims 3-5, 686 teaches that the switching elements 100 are interconnect in form of stack through interfaces 205 and 225 connected by a plurality of links 141. 686 does not teach that the cascading interface 225 includes an arbiter for allocating communication bandwidth between the first and second stacking port, and a flow control logic for controlling data flow to and from each of the first and second network switches. However, 196 teaches that a switch 100 comprises a cascading interface 108 connected with a shared memory manager 110 including a buffer memory controller (BMC) 112; see fig. 1. The BMC 112 comprises an arbiter 210 and an arbiter/scheduler 214 (see fig. 2) in order to allocate bandwidth and control data rate for fast ports 222 and slow ports 202. Therefore, it implies that the BMC 112 performs the functions as recited in claims 3-5. However, 196 does not teach that the BMC 112

located at the interfaces 106 and 108. *See In re Japikse, 86 USPQ 70 (CCPA 1950)*. It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the bandwidth allocating method disclosed by 196 into 686's system for utilizing the bandwidth of the system in order to maximize data transmission through the system.

Regarding claim 6, 686 does not disclose that the system forwards data packets to the egress ports without requiring a lookup in an address table. However, 196 discloses that the system comprises arbiters to determine output port based on an access request of the data packets, abstract, figs. 2-4; col. 1, line 57 – col. 2, line 6; col. 3, line 46 – col. 4, line 31. Therefore, it indicates that the system does not comprise a lookup table to determine output ports for the data packets. It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the method disclosed by 196 into 686's system in order to simplify for reducing the cost of the system.

Response to Arguments

Applicants' arguments filed 11/08/2005 have been fully considered but they are not persuasive.

Regarding claims 1 and 7, page 7 of the remarks, Applicants argue that Muller does not teach or suggest the limitation "wherein the first switch adds a module header having module identifier fields, providing a source module ID of the first switch, to the incoming packets and the second stacking port reads the module header to determine egress ports for the packets," Examiner respectfully disagrees. Since switches in the

Muller's system are Ethernet packet switches (col.4, lines 44-53); therefore, each of the switch elements 100 in the system shown in figure 1 adds to each of the incoming data packets a Ethernet packet header, which comprises a plurality of header fields, such as source address, destination address, port, IP address.... The switch determines egress port for routing the data packets to a destination according to the information of the headers; col. 13, lines 9-22 as explained in the claim 1 set forth in this office action.

Page 8, first paragraph, Applicants show the differences between the module header of the present application and a generic header. However, Examiner believes that this argument is not relevant because it is directed to subject matter not found in the claims 1 and 7.

Page 8, second paragraph, Applicants argue the reference "fails to teach or suggest adding a header to an incoming packet." Examiner respectfully disagrees. Since the switches in the system disclosed by Muller are packet switches. In any packet switch, each transmitting or receiving data packet comprises a payload portion (data) and a header portion (information of the packet), wherein the header is generated and added to the data packet by a switch. Thus, Muller's system comprises the step of adding a header into an incoming data packet as recited in claims 1 and 7.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai D. Hoang whose telephone number is (571) 272-3184. The examiner can normally be reached on Monday-Friday 10:00am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (571) 272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thai Hoang

CHI PHAM
SUPERVISORY PATENT EXAMINER
1/18/06